Exhibit 13

DDR5 SDRAM UDIMM Core

Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.1V (V_{DD}) double data rate, synchronous DRAM, unbuffered memory modules (DDR5 SDRAM UDIMMs). These DDR5 UDIMMs are intended for use as main memory when installed in PCs. Some specifications are part number-specific; refer to the module data sheet addendum of the specific Micron part number (MPN) for the complete specification.

Features

- DDR5 functionality and operations supported as defined in the component data sheet
- 288-pin UDIMM
- Sideband access with I3C-basic/I2C support
- Two independent I/O sub channels for increased bandwidth
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated clock, control and command/address bus

Table 1: Product Family Attributes

Parameter	Options	Notes
DIMM organization	x64, x72 ECC	Two 32-bit sub-channels (non-ECC), two 36-bit sub-channels (ECC)
DIMM dimensions (nominal)	133.35mm x 31.25mm	Refer to Module Dimensions
Pin count	288	
DDR5 SDRAM densities supported	16Gb, 24Gb, 32Gb, 64Gb	78/82-ball FBGA package for x4/x8 devices
Capacity	8Gb–128GB	
DDR5 SDRAM width	x8, x16	
Data transfer rate	PC5-3200 to PC5-5600	Refer to Key Timing Parameters
Serial presence detect hub with temperature sensor	1024 byte	
Voltage (external supply, nominal)	V_{IN_Bulk}: 5V	Bulk input DC supply voltage from system
Voltage (PMIC output)	V_{DD}: 1.1V	Supply voltage from PMIC
	V_{DDQ}: 1.1V	I/O Supply voltage from PMIC
	V_{PP}: 1.8V	Pump voltage from PMIC
	1.8V LDO output	From PMIC to HUB
	1.0V LDO output	
Interface	1.1V signaling	
DRAM operating temperature	T_{OPER} = 0 to 95°C	Refer to Thermal Characteristics

Notes: 1. Attributes shown in this table are for reference only and do not necessarily reflect the same options supported by Micron. Please refer to the MPN-specific module addendum for supported features for the MPN.

Table 2: Key Timing Parameters[1]

Speed Grade	PC5	Data Rate (MT/s) CL =												^{t}AA (ns)	^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		50	46	42	40	38	36	34	32	30	28	26	22				
56B	5600	5600	5600/ 5200	5200	4800/ 4400	–	4400/ 4000	–	4000/ 3600	3600	3200	3200	2100	16.000	16.000	16.000	48.000
52B	5200	–	5200	5200	4800/ 4400	–	4400/ 4000	–	4000/ 3600	3600	3200	3200	2100	16.000	16.000	16.000	48.000
48B	4800	–	–	4800	4800/ 4400	–	4400/ 4000	–	4000/ 3600	3600	3200	3200	2100	16.000	16.000	16.000	48.000

Notes: 1. ^{t}AA, ^{t}RCD, ^{t}RP and ^{t}RC values represent the tightest capability across all supported data rates and CL combinations. Refer to component data sheet Speed Bin Tables for details.

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General Description

High-speed DDR5 SDRAM modules use DDR5 SDRAM devices with four or eight internal memory bank groups. DDR5 SDRAM modules utilizing 4- and 8-bit-wide DDR5 SDRAM devices have eight internal bank groups consisting of four memory banks each, providing a total of 32 banks. 16-bit-wide DDR5 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of sixteen banks. DDR5 SDRAM modules benefit from DDR5 SDRAM's use of an 16*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR5 SDRAM effectively consists of a single 16*n*-bit-wide, eight-clock data transfer at the internal DRAM core and sixteen corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR5 modules use two sets of differential signals (DQS_t and DQS_c) to capture data, and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR5 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be accounted for by using the write-leveling feature of DDR5.

Pin Assignments

The pin assignment table below is a comprehensive list of all possible pin assignments for DDR5 UDIMM modules. Certain pins may not apply for a specific part number. Refer to the functional block diagram in the module data sheet addendum for a specific MPN.

Table 3: Pin Assignments

288-Pin DDR5 UDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V_{SS}
2	RFU	38	V_{SS}	74	V_{SS}	110	DQ5_B
3	RFU	39	DQ21_A	75	RFU	111	V_{SS}
4	HSCL	40	V_{SS}	76	RFU	112	DQ8_B
5	HSDA	41	DQ24_A	77	V_{SS}	113	V_{SS}
6	V_{SS}	42	V_{SS}	78	CK0_B_t	114	DQ9_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	V_{SS}
8	V_{SS}	44	V_{SS}	80	V_{SS}	116	DM1_B_n
9	DQ0_A	45	DM3_A_n	81	RFU	117	V_{SS}
10	V_{SS}	46	V_{SS}	82	CA12_B	118	DQ12_B
11	DQ1_A	47	DQ28_A	83	V_{SS}	119	V_{SS}
12	V_{SS}	48	V_{SS}	84	CA10_B	120	DQ13_B
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	V_{SS}
14	DQS0_A_t	50	V_{SS}	86	V_{SS}	122	DQ16_B
15	V_{SS}	51	CB0_A	87	CA6_B	123	V_{SS}
16	DQ4_A	52	V_{SS}	88	CA4_B	124	DQ17_B
17	V_{SS}	53	CB1_A	89	V_{SS}	125	V_{SS}
18	DQ5_A	54	V_{SS}	90	CA2_B	126	DQS2_B_c
19	V_{SS}	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t
20	DQ8_A	56	DQS4_A_t	92	V_{SS}	128	V_{SS}
21	V_{SS}	57	V_{SS}	93	CS0_B_n	129	DQ20_B
22	DQ9_A	58	CS0_A_n	94	V_{SS}	130	V_{SS}
23	V_{SS}	59	V_{SS}	95	RESET_n	131	DQ21_B
24	DM1_A_n	60	CA0_A	96	V_{SS}	132	V_{SS}
25	V_{SS}	61	CA2_A	97	CB0_B	133	DQ24_B
26	DQ12_A	62	V_{SS}	98	V_{SS}	134	V_{SS}
27	V_{SS}	63	CA4_A	99	CB1_B	135	DQ25_B
28	DQ13_A	64	CA6_A	100	V_{SS}	136	V_{SS}
29	V_{SS}	65	V_{SS}	101	DQ0_B	137	DM3_B_n
30	DQ16_A	66	CA8_A	102	V_{SS}	138	V_{SS}
31	V_{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B
32	DQ17_A	68	V_{SS}	104	V_{SS}	140	V_{SS}
33	V_{SS}	69	CA12_A	105	DQS0_B_c	141	DQ29_B
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	V_{SS}
35	DQS2_A_t	71	V_{SS}	107	V_{SS}	143	RFU

288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	V_{SS}
146	VIN_BULK	182	V_{SS}	218	V_{SS}	254	DQ7_B
147	PWR_-GOOD	183	DQ23_A	219	RFU	255	V_{SS}
148	HSA	184	V_{SS}	220	RFU	256	DQ10_B
149	RFU	185	DQ26_A	221	V_{SS}	257	V_{SS}
150	V_{SS}	186	V_{SS}	222	CK1_B_t	258	DQ11_B
151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	V_{SS}
152	RFU	188	V_{SS}	224	V_{SS}	260	DQS1_B_c
153	V_{SS}	189	DQS3_A_c	225	RFU	261	DQS1_B_t
154	DQ2_A	190	DQS3_A_t	226	RFU	262	V_{SS}
155	V_{SS}	191	V_{SS}	227	V_{SS}	263	DQ14_B
156	DQ3_A	192	DQ30_A	228	CA11_B	264	V_{SS}
157	V_{SS}	193	V_{SS}	229	CA9_B	265	DQ15_B
158	DM0_A_n	194	DQ31_A	230	V_{SS}	266	V_{SS}
159	V_{SS}	195	V_{SS}	231	CA7_B	267	DQ18_B
160	DQ6_A	196	CB2_A	232	CA5_B	268	V_{SS}
161	V_{SS}	197	V_{SS}	233	V_{SS}	269	DQ19_B
162	DQ7_A	198	CB3_A	234	CA3_B	270	V_{SS}
163	V_{SS}	199	V_{SS}	235	CA1_B	271	DM2_B_n
164	DQ10_A	200	ALERT_n	236	V_{SS}	272	V_{SS}
165	V_{SS}	201	V_{SS}	237	CS1_B_n	273	DQ22_B
166	DQ11_A	202	CS1_A_n	238	V_{SS}	274	V_{SS}
167	V_{SS}	203	V_{SS}	239	DQS4_B_c	275	DQ23_B
168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	V_{SS}
169	DQS1_A_t	205	CA3_A	241	V_{SS}	277	DQ26_B
170	V_{SS}	206	V_{SS}	242	CB2_B	278	V_{SS}
171	DQ14_A	207	CA5_A	243	V_{SS}	279	DQ27_B
172	V_{SS}	208	CA7_A	244	CB3_B	280	V_{SS}
173	DQ15_A	209	V_{SS}	245	V_{SS}	281	DQS3_B_c
174	V_{SS}	210	CA9_A	246	DQ2_B	282	DQS3_B_t
175	DQ18_A	211	CA11_A	247	V_{SS}	283	V_{SS}
176	V_{SS}	212	V_{SS}	248	DQ3_B	284	DQ30_B
177	DQ19_A	213	RFU	249	V_{SS}	285	V_{SS}
178	V_{SS}	214	RFU	250	DM0_B_n	286	DQ31_B
179	DM2_A_n	215	V_{SS}	251	V_{SS}	287	V_{SS}

Table 3: Pin Assignments (Continued)

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
36	V_{SS}	72	CK0_A_t	108	DQ4_B	144	RFU	180	V_{SS}	216	CK1_A_t	252	DQ6_B	288	RFU

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR5 UDIMM/SODIMM devices. All pins listed may not be supported on a specific module. See Functional Block Diagram in the MPN-specific addendum for pins applicable to a given module.

Table 4: Pin Descriptions

Symbol	Type	I/O Level	Description
CK[1:0]_A_t, CK[1:0]_B_t, CK[1:0]_A_c, CK[1:0]_B_c	Input	V_{DDQ}	**SDRAM Clocks** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[12:0]_A CA[12:0]_B	Input	V_{DDQ}	**Command/Address Inputs:** CA signals provide the command and address inputs according to the Command Truth Table. Note that because some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands. The DDR5 component CA13 pin is strapped (connected) to either V_{SS} or V_{DDQ} depending on the strapped state of MIR.
CS[1:0]_A CS[1:0]_B	Input	V_{DDQ}	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and V_{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD}.
ALERT_n	Output	V_{DDQ}	**Alert:** If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to V_{DDQ} on the system board.
RESET_n	CMOS Input	V_{DDQ}	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ}.
PWR_GOOD	Input Output	V_{DDQ}	**Power Good Indicator:** Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Clock:** Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Data:**I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.

Table 4: Pin Descriptions (Continued)

Symbol	Type	I/O Level	Description
HSA	Input	GND	**Host Sideband Bus Device ID:** Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
DQ[31:0]_A DQ[31:0]_B	Input/ Output	V_{DDQ}	**Data Input/Output:** Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0–DQ3 may indicate the internal V_{REF} level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB[3:0]_A CB[3:0]_B	Input/ Output	V_{DDQ}	**ECC Check Bits Input/Output:** Bidirectional data bus. Only applicable on ECC SODIMM (SOEDIMM) or UDIMM (EUDIMM).
DQS[4:0]_A_t DQS[4:0]_B_t DQS[4:0]_A_c DQS[4:0]_B_c	Input/ Output	V_{DDQ}	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DM[3:0]_A_n DM[3:0]_B_n	Input	V_{DDQ}	**Input Data Mask:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM function is shared with TDQS on x8 devices. The function of DM_n is enabled by MR5:OP[5] = 1. Refer to Micron DDR5 component data sheet specification for further detail.
VIN_BULK	Supply		**External Power Supply:** 5V, 4.25V (min), 5.5V (max)
PWR_EN	Input		**PMIC Enable:** When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
V_{SS}	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			**No connect:** No internal electrical connection is present.
NF			**No function:** May have internal connection present, but has no function.

Address Mapping to DRAM

Address Mirroring

DDR5 SDRAM has an MIR input pin. This pin is strapped (connected) to V_{SS} or V_{DDQ} on the PCB. This pin is used to inform the SDRAM device that it is being configured for mirrored mode vs. standard mode. With the MIR pin strapped to V_{DDQ}, the SDRAM internally swaps even-numbered CA with the next higher odd number CA. Normally, the MIR pin must be strapped to V_{SS} if no CA mirror is required. The following table illustrates how the edge connector pin maps to the DRAM physical CA pins and internal CA function.

Table 5: Address Mirroring

Edge Connector Pin	Unmirrored DRAM (MIR = V_{SS})[1]		Mirrored DRAM (MIR = V_{DDQ})[2]	
	Physical Pin Connected	Internal Function	Physical Pin Connected	Internal Function
CA0	CA0	CA0	CA1	CA0
CA1	CA1	CA1	CA0	CA1
CA2	CA2	CA2	CA3	CA2
CA3	CA3	CA3	CA2	CA3
CA4	CA4	CA4	CA5	CA4
CA5	CA5	CA5	CA4	CA5
CA6	CA6	CA6	CA7	CA6
CA7	CA7	CA7	CA6	CA7
CA8	CA8	CA8	CA9	CA8
CA9	CA9	CA9	CA8	CA9
CA10	CA10	CA10	CA11	CA10
CA11	CA11	CA11	CA10	CA11
CA12	CA12	CA12	CA13	CA12

Notes: 1. On the side of the DIMM which has the MIR pin strapped to V_{SS}, the DRAM's CA13 pin is strapped to V_{DDQ}.
2. On the side of the DIMM which has the MIR pin strapped to V_{DDQ}, the DRAM's CA12 pin is strapped to V_{DDQ}.

SPD EEPROM Hub and Integrated Thermal Sensor Operation

SPD EEPROM Hub Operation

DDR5 SDRAM modules incorporate an SPD EEPROM with hub function (SPD5 Hub) with integrated thermal sensor (TS). The SPD data is stored in a 1024-byte, JEDEC JC-42.4-compliant EEPROM that is arranged as 16 blocks of 64 bytes per block, and each block may optionally be write-protected via software command. The SPD content is aligned with these blocks, as shown in the table below.

Block	Range		Description
0	0~63	0x000~0x03F	Base configuration and DRAM parameters
1	64~127	0x040~0x07F	Base configuration and DRAM parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See annex A.0 for details
	240~255	0x0D0~0x0FF	Standard module parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard module parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard module parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard module parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FF	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for SPD bytes 0~509
8	512~575	0x200~0x23F	Manufacturing information
9	576~639	0x240~0x27F	Manufacturing information
10	640~703	0x280~0x2BF	End user programmable
11	704~767	0x2C0~0x2FF	End user programmable
12	768~831	0x300~0x33F	End user programmable
13	832~895	0x340~0x37F	End user programmable
14	896~959	0x380~0x3BF	End user programmable
15	960~1023	0x3C0~0x3FF	End user programmable

The first 640 bytes are programmed by Micron to comply with JEDEC standard JESD400-5, "DDR5 Serial Presence Detect (SPD) Contents." The remaining 384 bytes of storage are available for use by the end user.

The EEPROM resides on a two-wire I3C serial interface, which is also compatible with legacy I2C interface and is not integrated with the memory bus in any manner. It operates as an initiator/target device in the I3C-basic protocol, with all operations synchronized by the serial clock. Transfer rates of up to 12.5 MHz are achievable at 1.0V (NOM).

Micron implements reversible software write protection on DDR5 SDRAM-based modules. This prevents the lower 640 bytes (bytes 0 to 639) from being inadvertently programmed or corrupted. The upper 384 bytes remain available for customer use and are unprotected.

Integrated Thermal Sensor Operations

The integrated thermal sensor (TS) continuously monitors the temperature of the module PCB and updates the temperature data register. Temperature data may be read from the bus host at any time, which provides the host real-time feedback of the module's temperature. Multiple programmable and read-only temperature registers can be used to create a custom temperature-sensing solution based on system requirements and JEDEC JC-42.2. Refer to the DDR5 SPD5 Hub spec for detailed information on configuring and reading the integrated thermal sensor.

Power Management Integrated Circuit Operation

The power management integrated circuit (PMIC) is new for DDR5. JEDEC defines the PMIC5100 device for DDR5 UDIMMs and SODIMMs. This operation converts a 5V supply into regulated values for all components on the module. The PMIC5100 has ~10.6W of average output power capability. The PMIC5100 utilizes a unique pinout and 3mm x 4mm FCQFN package. The PMIC also allows the host to monitor voltage and current via the sideband channel. Refer to JEDEC JESD301-2 "PMIC5100 Power Management IC Specification" for full details.

The PMIC5100 has one 5V nominal supply input pin from the card edge through VIN_Bulk. The PMIC has the ability to regulate lower voltages to the HUB which allows external access to read/configure this device prior to the VR ENABLE command. The VIN_Bulk supply, after the VR ENABLE command, will supply all regulated voltages to the PMIC and DRAM.

The PMIC allows the DIMM manufacturer to set the target voltage levels for the DRAM and configure the ramp up and ramp down aspects of each power rail. For power up, each voltage rail can be configured in offsets of 2ms increments and for power down in increments of 1ms. Note, there will be independent power planes for all UDIMM and SODIMM layouts. The DRAM will be connected to all three rails (V_{DD}, V_{DDQ} and V_{PP}).

The PMIC has a PWR_GOOD pin, which is an Open Drain and will have an external pull-up. The functionality of the PWR_GOOD pin is configurable as an input/output pin. When the VIN_Bulk input reaches valid threshold levels, the PMIC will float PWR_GOOD pin indicating a successful initialization. At this time the PMIC releases the PWR_GOOD signal and allows it to float HIGH (external pull-up resistor on the host side will pull it HIGH). At any time thereafter if VIN_Bulk drops below a set threshold, or any of the regulated supplies fall out of specification, the PMIC will drive the PWR_GOOD signal LOW to flag the host. The VR ENABLE command or pin, when set HIGH, will enable the regulators which control all DRAM voltages are stable; when set LOW, it will disable all output regulators.

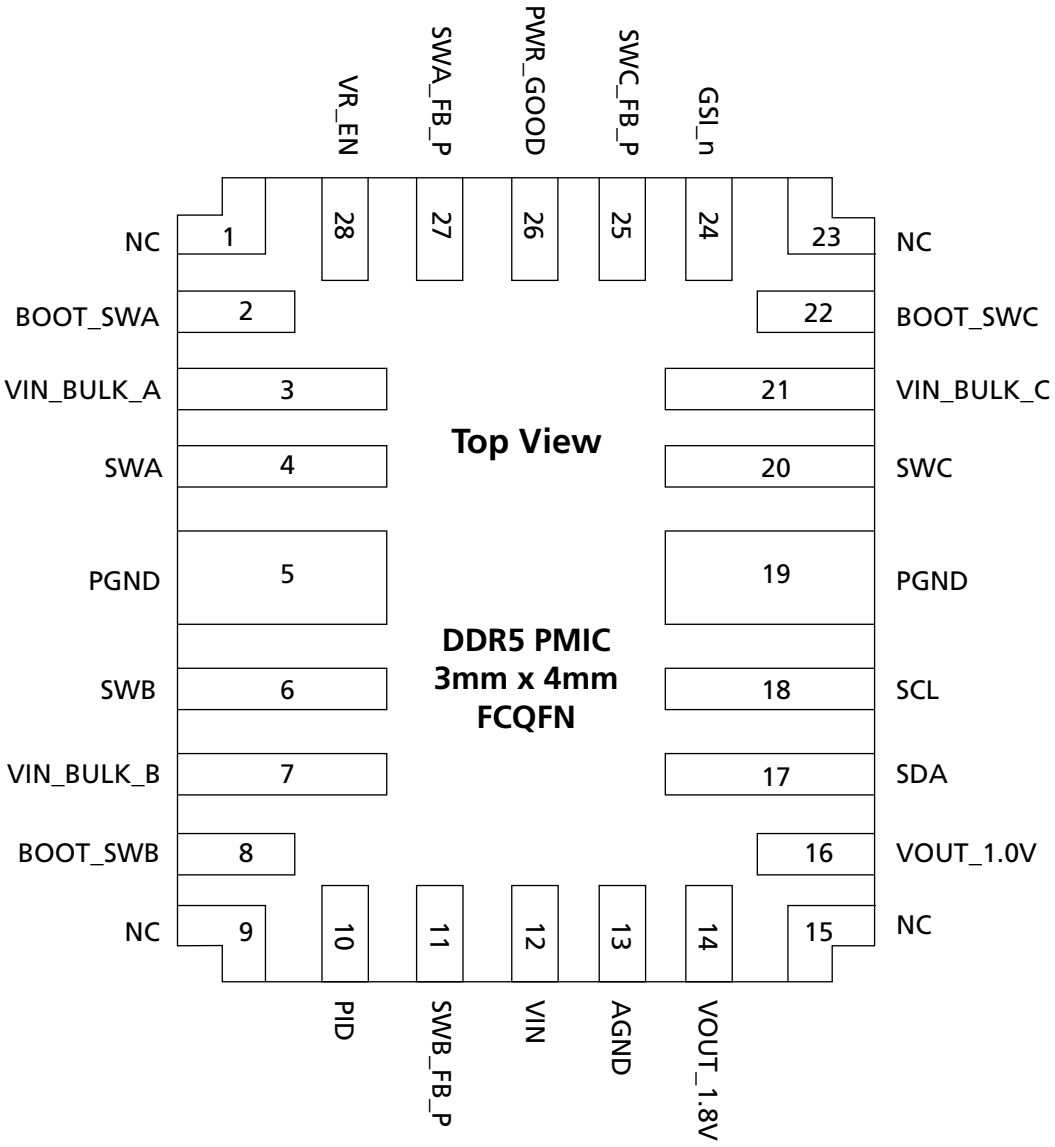
By default, the PMIC powers up in I2C mode, and the host can reconfigure to support I3C-basic if needed. There are three address configurations for the PMIC Address ID (PID), device pin #10. See the table below for options.

Table 6: PMIC Addressing

PID Configuration (Pin #13)	PMIC Address ID (PID)			
	Bit 7	Bit 6	Bit 5	Bit 4
Pin to V_{SS}	1	0	0	1
Pin to 1.8V	1	1	0	0
Pin Floating	1	0	0	0

The PMIC has multiple sets of registers, primarily the DIMM vendor region and the host region. The vendor region is used to set up the voltage ramps, supply rail values, and threshold settings. The host can also set various registers to flag critical operation conditions and to help debug. After the VR_ENABLE command is issued, the PMIC can only be programmed in a non-secure mode. If the device remains in a secure mode after the VR_ENABLE command, the device locks out the ability to change the contents of most registers.

Figure 1: PMIC Package



Thermal Characteristics

Table 7: DDR5 SDRAM Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	DRAM Commercial operating case temperature	0 to 85	°C	1, 2, 3
T_C		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	DRAM operating temperature range	0 to 95	°C	5, 7, 8
T_{STG}	DRAM Non-operating storage temperature	–55 to 100	°C	6

Notes: 1. Maximum operating case temperature; T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. The refresh rate must double when 85°C < T_C ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.
7. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C and 85°C under all operating conditions for the commercial offering.
8. For additional information, refer to technical note TN-00-08: "Thermal Applications" available at micron.com.

DDR5 Module Capacitor Operating Temperature

Micron DDR5 SDRAM Modules use X5R capacitors which are limited to a maximum operating case temperature rating of 85C. All other components on the DIMM meet or exceed the DDR5 SDRAM maximum commercial operating case temperature rating of 95C. The JEDEC DIMM design specifications require all non-DRAM components are maintained within their respective operating temperature ratings when the case temperature of the DRAMs are at their minimum and maximum specified values.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR5 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

Table 8: Module and Component Speed Grades

DDR5 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
56B	-56B
52B	-52B
48B	-48B

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

DRAM operating voltages are generated by an on-DIMM PMIC component. Power to the PMIC is provided through the VIN_BULK (12V for RDIMMs and LRDIMMs, 5V for UDIMMs and SODIMMs) and 3.3V VIN_MGMT (LRDIMMs and RDIMMs only) edge connector pins. Designers must account for any system voltage drops at anticipated power levels to ensure the required VIN supply voltage is maintained.

SPD EEPROM Hub and Integrated Thermal Sensor Operating Conditions

The thermal sensor continuously monitors the module's temperature and can be read back at any time over the sideband bus shared with the serial presence-detect (SPD) EEPROM. Refer to JESD300-5 SPD5118 device specification for complete details.

SPD Data

For the latest SPD data, refer to Micron's SPD page: micron.com/SPD.

Table 9: SPD EEPROM Hub and Integrated Thermal Sensor Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	V_{DDSPD}	1.7	1.8	1.98	V
Supply voltage	V_{DDIO}	0.95	1.0	1.05	V
Input low voltage	V_{IL}	–0.35	–	0.3	V
Input high voltage	V_{IH}	0.7	–	3.6	V
Output low voltage	V_{OL}	–	–	0.3	V
Output high voltage	V_{OH}	0.75	–	–	
Input leakage current	I_{LI}	–	–	±5	µA
Output leakage current	I_{LO}	–	–	±5	µA

Table 10: Temperature Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	I2C Mode - Open Drain		I3C Basic Push-Pull		Units
		Min	Max	Min	Max	
Clock frequency	^{f}SCL	0.01	1	0	12.5	MHz
Clock pulse width HIGH time	$^{t}HIGH$	260	–	35	–	ns
Clock pulse width LOW time	^{t}LOW	500	–	35	–	ns
Detect clock LOW timeout	$^{t}TIMEOUT$	10	50	10	50	ns
SDA rise time	^{t}R	–	120	–	5	ns
SDA fall time	^{t}F	–	120	–	5	ns
Data-in setup time	$^{t}SU:DAT$	50	–	8	–	ns
Data-in hold time	$^{t}HD:DI$	0	–	3	–	ns
Data out hold time	$^{t}HD:DAT$	0.5	350	N/A	N/A	ns
Start condition setup time	$^{t}SU:STA$	260	–	12	–	ns
Start condition hold time	$^{t}HD:STA$	260	–	30	–	ns
Stop condition setup time	$^{t}SU:STO$	260	–	12	–	ns
Time the bus must be free before a new transition can start	^{t}BUF	500	–	500	–	ns
Write time	^{t}W	–	5	–	5	ms

Table 10: Temperature Sensor and EEPROM Serial Interface Timing (Continued)

Parameter/Condition	Symbol	I2C Mode - Open Drain		I3C Basic Push-Pull		Units
		Min	Max	Min	Max	
Warm power cycle time off	$^{t}POFF$	1	–	1	–	ms
Time from power-on to first command	$^{t}INIT$	10	–	10	–	ms

Power Management Integrated Circuit Operating Conditions

Due to the PMIC capability, 5V is the nominal supply to the PMIC from the host through the edge connector pins. The output voltage levels from the PMIC are expected to operate within ± 52.5% in order to satisfy the DRAM voltage requirement range of -3% to +6%.

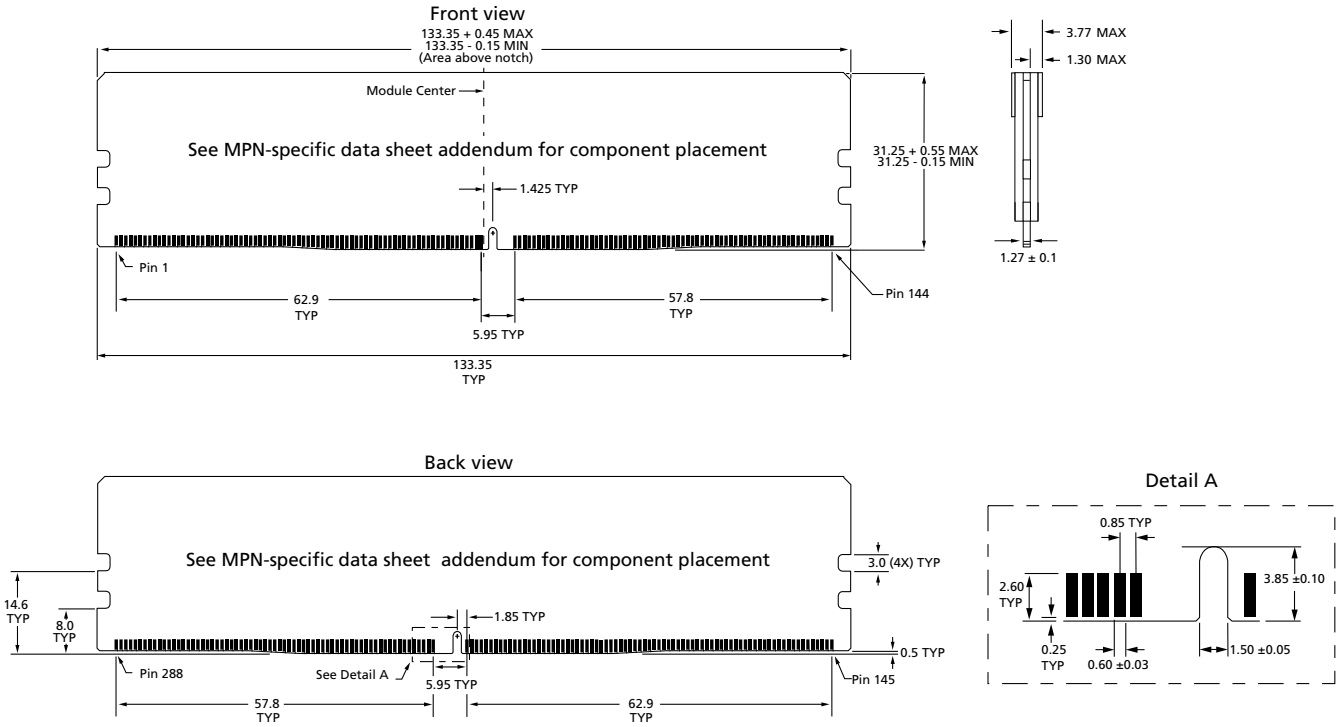
Table 11: PMIC 5100 Input Supply Electrical Characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Bulk input supply voltage	VIN_Bulk	4.25	5.0	5.5	V	2
Bulk input supply maximum – AC voltage	VIN_Bulk_AC	–	–	6.5	V	
Bulk input supply voltage – ramp up rate	VIN_Bulk_Ramp_Up	0.1	–	3.0	V/ms	3
Bulk input supply voltage – ramp down rate	VIN_Bulk_Ramp_Down	0.5	–	1.0	V/ms	4
Bulk input supply voltage – start up overshoot	VIN_Bulk_OS_Startup	–	–	TBD	V*µs	5
Maximum input current for VIN_Bulk input supply voltage	I_{VIN_Bulk}	0.05	–	2.0	A	6
VIN_Bulk Input Quiescent Current	$I_{VIN\_Bulk\_Quiescent}$	–	–	25	µA	7
VIN_Bulk Input Idle Current	$I_{VIN\_Bulk\_Idle}$	–	–	TBD	µA	8

Notes: 1. Input supplies referenced in this table are VIN_BULK and VIN.
2. During first power-on, the input voltage supply must reach a minimum of 4.25V for the PMIC to detect a valid input supply.
3. The ramp up rate is between 300mV and 4.0V.
4. The ramp down rate is between 4.0V and 300mV.
5. The area under the curve and above VIN_Bulk = TBD. The VIN_Bulk_AC spec must also be satisfied.
6. The minimum input current requirement is equal to the maximum output current on VOUT_1.8V and VOUT_1.0V LDO, plus the current required by the PMIC for its own use. The maximum input current is equal to the all VIN_Bulk input on the PMIC.
7. VIN_Bulk = 5.0V measured at room temperature. All circuitry, including output regulators and LDOs are off. The VR_EN signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I^2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW.
8. VIN_Bulk = 5.0V measured at room temperature. All output regulators and LDOs are on the 0A output load. The VR_EN signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I^2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW.

Module Dimensions

Figure 2: 288-Pin DDR5 UDIMM



Notes: 1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15 unless otherwise specified.
3. The dimensional diagram is for reference only.

Revision History

Rev. E – 10/2021

- Remove Micron Confidential marking

Rev. D – 08/2021

- Production Release

Rev. C – 02/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.